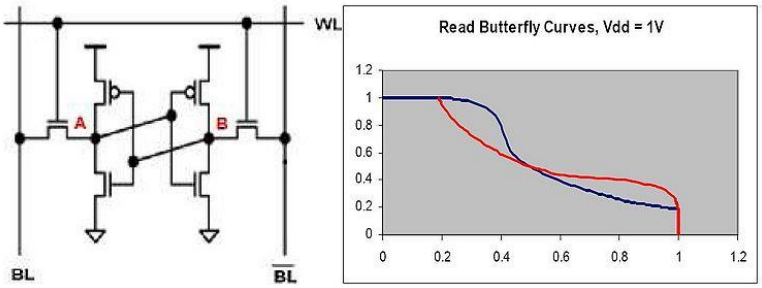
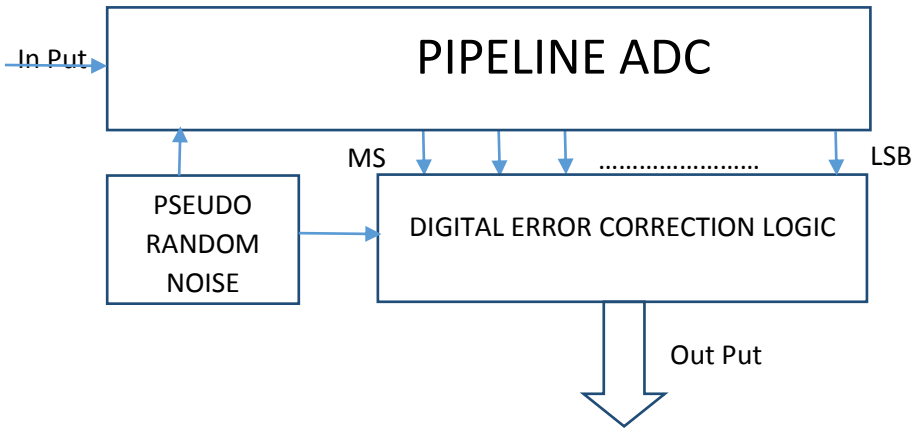
Student Details	Project Details
 A. VENKATA REDDY **Contact : 7030968957** **Email**: reddyvenkat59@gmail.com **Areas of Interest**: Memory design & Memory Layout, Analog Design, Front End Design	**Title:** **Read Margin Improved 6T SRAM cell Design and Leakage power Reduction using Multi-Threshold MOS** **Abstract:** 6T-SRAM can be optimized for stability by choosing the cell layout, device threshold voltages, and the ß ratio. Process variation effects width to length ratio and threshold voltage, stability may reduce due to these variations. SRAM cell stability will be a primary concern for future technologies due to variability and decreasing power supply voltages. Proposed 6T-SRAM however, provides a much greater enhancement in stability by eliminating cell disturbs during a read access, thus facilitating continued technology scaling. Leakage power problem small in Conventional 6T compare to all other SRAM cells. Leakage power of proposed method is reduced by using Multi-Threshold voltage MOS Technique. So, Proposed technique eliminate needs of higher transistor number SRAM cells like 7T,8T and 9T. **Block Diagram:**  Modified above 6T transistor cell to get better read margin .
 ARJUN T V **Contact:8407962404** **Email**: arjunvasudevann@gmail.com **Areas of Interest**: Digital Background Calibration of Pipeline ADC	**Title:** **Digital Background Calibration of Pipeline ADC by Radix modification** **Abstract:** Pipeline analog-to-digital converters (ADCs) are integral part for applications demanding high resolution analog to digital conversion. The main challenge faced by this ADC are errors resulting from capacitor mismatches and finite op-amp gain and accumulation of these errors as the number of stages gets increased. In order to compromise these errors while keeping the normal ADC operation unaffected background calibration is performed by recalculating the digital output based on each stage's equivalent radix. The equivalent radices are extracted in the background by using a digital correlation method that makes use of a pseudo random noise pattern applied along with the signal to the ADC. And the extracted radices are used to calculate the corrected output. 

Ch.Yehoshuva

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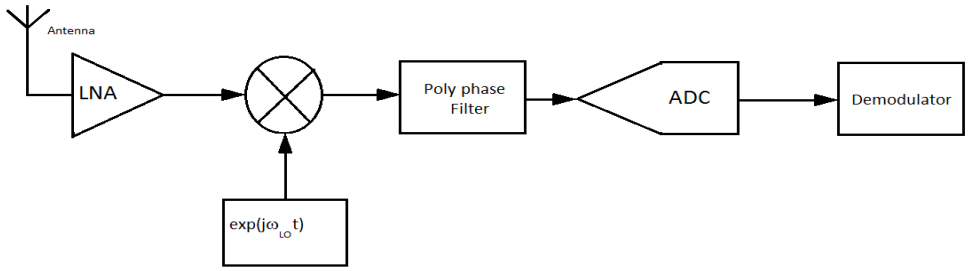
Areas of Interest: Analog Filter Design-Poly Phase Filter Design

Title:

CMOS Analog Poly Phase Filter Design for use in Rf Systems

Abstract:

Polyphase Filters or Complex filters are mainly used to remove image frequency in the receiver of Wireless communication Systems. The main Principle of these filters is to remove negative frequency. Though SAW filters by its huge Q-factor can be used to remove Image frequency but SAW filters cannot be used as on chip component it has to be off chip component which will increase the size of the system. Analog passive polyphse filters operated with power due to less gain the sensitivity of ADC which is next block of filter will be decreased Hence the High Gain CMOS polyphse filters are preferred.



HARIN GOLLA

Title:

K.Manikantta Reddy

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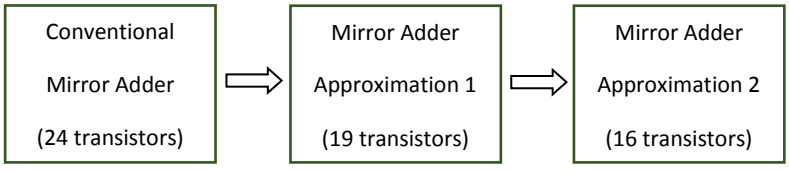
Areas of Interest: Low power and high speed digital circuit design

Title:

Design of Low Power, High Speed Multipliers Using Approximate Adders.

Abstract:

In most of the multimedia applications such as audio, speech, graphics and video the final output is interpreted by human senses, which are insensitive to small errors. So, it is not required to produce exact numerical outputs. Considering the advantage of relaxation in numerical accuracy, we will design several approximate multipliers for error tolerant applications by using approximate adders. Approximate adder is constructed by reducing the complexity at the transistor level. The power consumption is reduces due to decrease in the number of transistors and switched capacitance. Decrease in the number of series connected transistors, lead to shorter critical paths. Propagation delay is also reduces due to decrease in load capacitance.



M. Aditya

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Areas of Interest: Reversible logic

Title:

Synthesis of Reversible and Adiabatic Logic Circuits for Low-Power Applications

Abstract:

Reversible logic is an emerging research area. Implementation of Reversible logic is found in application of thermodynamics and adiabatic CMOS. Power dissipation is an important issue in modern technologies. Using the principles of adiabatic switching we realize low-power CMOS circuits. During logic operations there is a significant power dissipation in Conventional circuits because information bits are erased. The logic circuits that do not erase any information bits dissipate zero power dissipation theoretically. Power consumption can be reduced by controlling the current flow through the circuit. We make use of Dual-rail adiabatic logic which show decrease in average and differential power.

applications in Memory and Analog Design, Verilog Coding

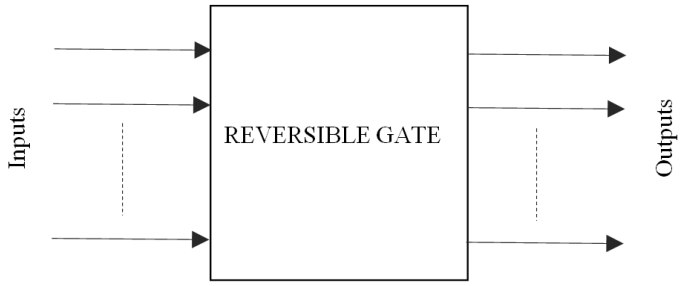

Fig. 1. Reversible gate with n-inputs and n-outputs

Mayur.S.Marinaik

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Areas of Interest: Digital design, Mixed Signal Design, Signal Processing.

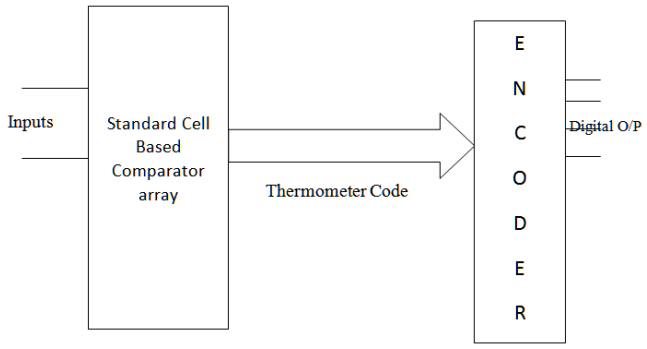
Title:

Design of Low Power 4 –Bit Flash ADC Based on Standard Cell Comparator and Multiplexer based encoder

Abstract:

In this paper, a standard cell low power 4-bit flash analog-to-digital converter (ADC) is proposed. The converter utilizes comparators created using only logic gates for converting analog input signals to digital values. This novel flash architecture consists of several CMOS gates with inputs connected to a common input node or to one of the supply lines. Depending on the relationship between the input signal and a given gate threshold voltage, the output will either be '0' or '1'.

The comparator is followed by an encoder to convert the thermometer code to binary code. In the proposed comparator the thermometer code is initially converted into intermediate gray code using 2:1 multiplexers and then to the binary code using XOR gates. The proposed architecture uses minimum number of multiplexers for the conversion and consumes less power. The proposed ADC is implemented at the transistor level in a 180nm CMOS technology with a 1.8 V supply voltage and is simulated using Cadence Spectre simulator.



4-Bit Flash ADC based on Standard cell comparator

Mohd Kashif Zia Ansari

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Areas of Interest: Memory Design,

Title:

A High Speed 8-bit Successive Approximation ADC.

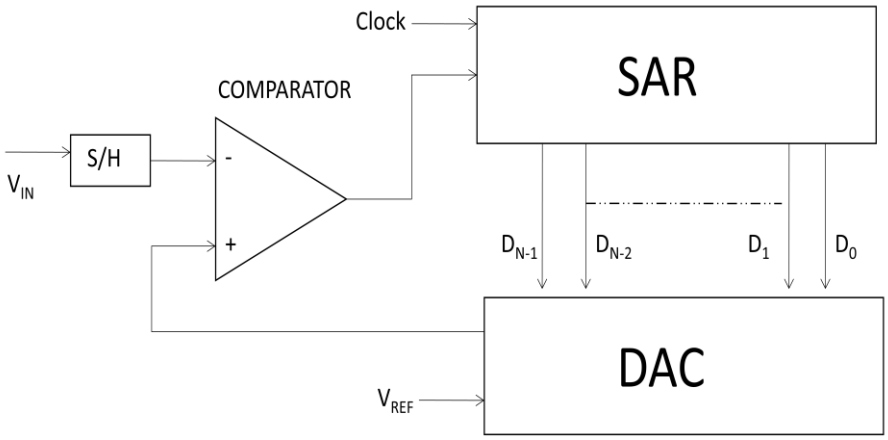
Abstract:

A SAR ADC is an analog-to-digital converter that converts a continuous analog waveform into a discrete digital representation. A SAR ADC uses an algorithm called *binary search* which compares the analog input to all the possible digital combinations, i.e. quantization levels to produce the digital outcome.

Though SAR ADC is a high resolution converter but the problem lies in its slowness. An *N*-bit SAR ADC would take *N* cycles to complete the conversion process.

Digital Circuit Design, Analog ADC, Verilog etc.

Hence, the idea is to overcome this sluggishness of SAR ADC by designing a modified SAR ADC



P.S.Veerendranath

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Areas of Interest: Low-power Analog design , Filter Design

Title:

A Wide Tuning Range G_m–C Continuous-time Analog Filter

Abstract:

This paper deals with tuning of continuous time analog filter. Now-a-days, There is a great demand for devices that operates for various applications. This exploits of saving chip area. In this tuning of a filter by varying the Transconductance. This can be varied by changing the bias current of OTA. The OTA can work from weak-inversion region to strong-inversion region to maximize the Transconductance.

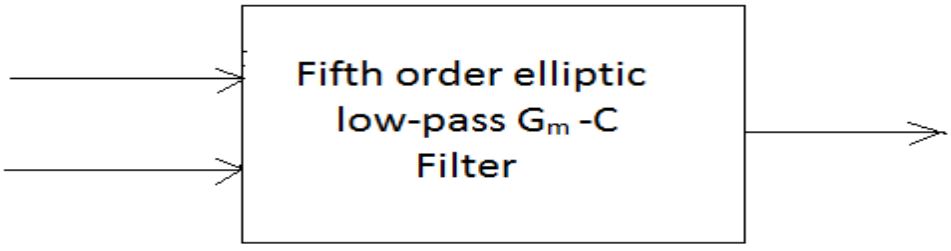

Fig: Fifth order elliptic low-pass G_m–C filter

SUJAL PATEL
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Title:

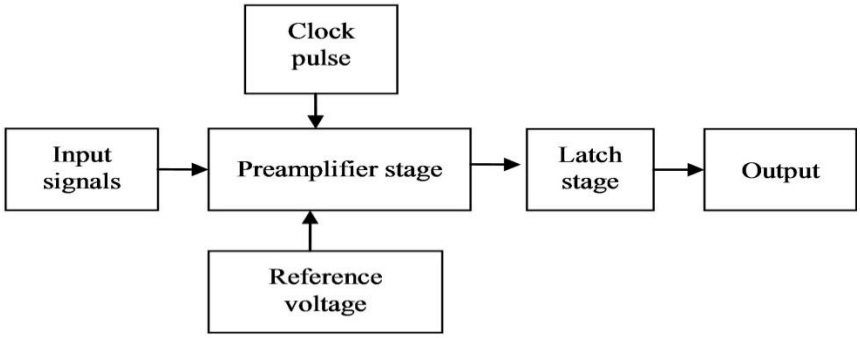
Low current consumption CMOS comparator using charge storage amplifier for A/D converter

Abstract:

A low-current consumption CMOS comparator using a charge-storage amplifier for A/D converters. A comparator is usually composed of an amplifier and a latch. Because the amplifier consumes higher amounts of current than the latch, the comparator needs a low-current consumption amplifier. In this paper, we propose a new charge storage amplifier for a low-current consumption comparator. The Charge-storage amplifier consumes a constant current only during the charging period to internal capacitors, which are used as load devices instead of transistors or resistors. The comparator was

Areas of Interest: Low current consumption CMOS comparator for A/D converter

Designed and fabricated using a standard logic CMOS technology. Consequently, the charge-storage amplifier consumed less than one-half of the current of a normal amplifier that had transistor Loads.



RHUSHIKESH JOSHI
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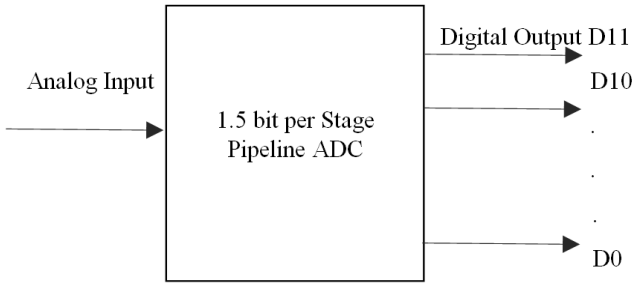
Areas of Interest: Mixed signal design, Semiconductor device modeling

Title:
Design of 1.5 bit per stage pipeline ADC with modified logic
Abstract:
Use of pipeline analog-to-digital converters (ADCs) continues to expand, both as standalone parts and as embedded functional blocks in system-on-a-chip (SoC) ICs. They form the most important part of mobile communication system. Pipelined converters attain their final resolution through a series cascade of lower-resolution stages.. Pipeline ADCs consist of a series of stages that are isolated by sample and hold (S/H) buffers. The stages work concurrently. The first stage operates on the most recent sample, while the following stages operate on analog remainder voltages, called residues from previous samples.. 1.5-bit stages in high speed pipelined ADCs have become established as both performance and cost-effective circuit blocks.



Pranose J Edavoor

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Areas of Interest: Multimedia processing,FPGA,Digital Design

Title:

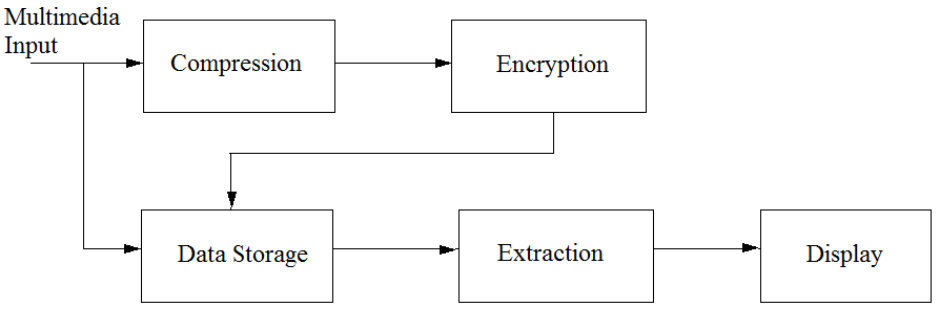
Realtime Multimedia compression and Encryption using FPGA

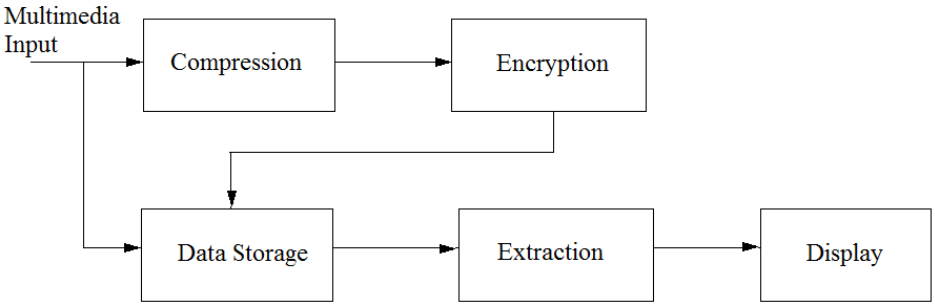
Abstract:

Realtime Multimedia processing is implemented using compression and encryption to optimize the total data to only the relevant data to represent images or video.

The project aims at processing realtime data.This is implemented using hardware description language Verilog and realized on Xilinx FPGA.An LUT based control logic is used for Distributive arithmetic unit used in the project.

Block Diagram:





S.Ahish

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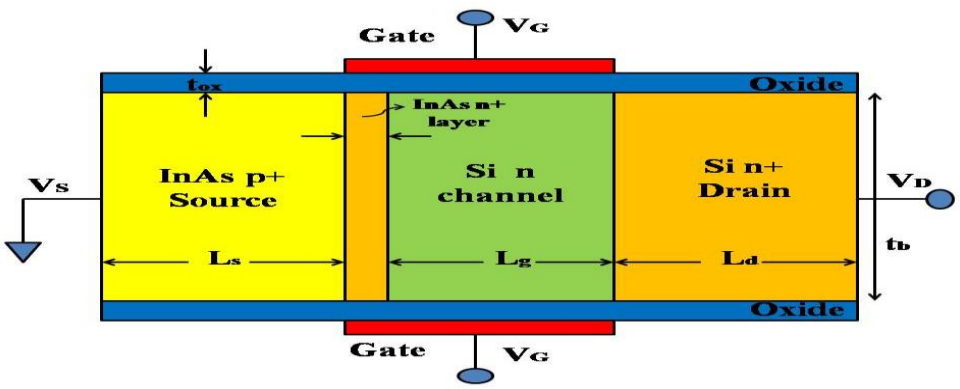
Areas of Interest: Device Modeling, Analog Design, and Verilog Coding.

Title:

Performance enhancement of heterojunction tunnel field effect transistor using Gaussian Doping Profile

Abstract:

In this paper, for the first time, DC characteristics and analog/RF performance of Hetero Junction Double-Gate Tunnel Field Effect Transistor (H-DGTFET) have been analyzed for uniform and gaussian doping profile. For this purpose, the threshold voltage of the device has been obtained by using transconductance change method and constant current method. Further, the effect of uniform and gaussian drain doping profile on analog/RF performance of H-DGTFET is investigated. A highly doped layer is placed in the channel near the source-channel junction, this results in the decrease in the width of the depletion region improving the ON-current (ION). It also improves the RF performance of the H-DGTFET. Also, the effect of uniform and gaussian doping profiles are analysed for different channel lengths. So, DC characteristics and analog/RF figures of merit for H-DGTFET is analyzed in terms of threshold voltage, current voltage characteristics, Subthreshold Slope (SS), transconductance (gm), gate to source capacitance (Cgs), gate to drain capacitance (Cgd), output resistance, current gain, cutoff frequency (fT) and gain bandwidth product (GBW). The simulations presented in this paper were carried out by using 2-D ATLAS.



Samir kumar

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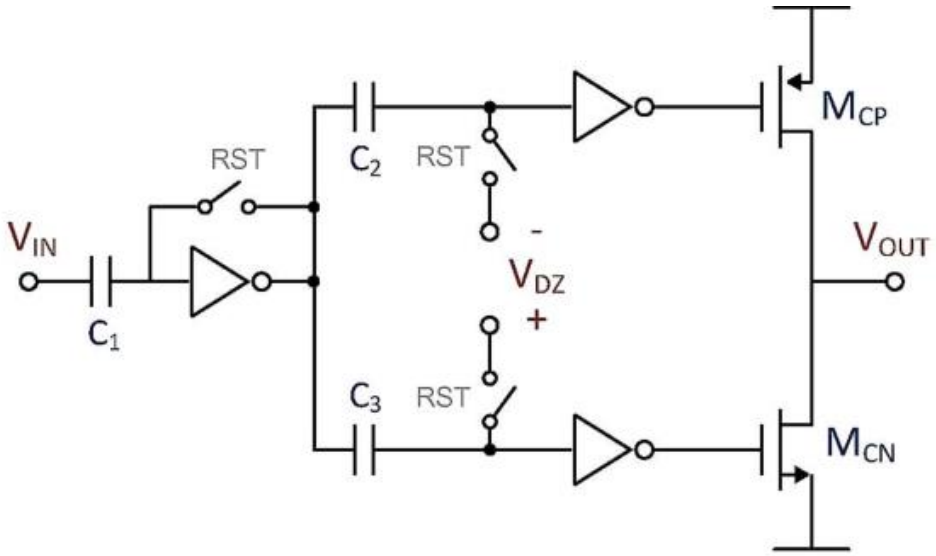
Areas of Interest: Ring amplifiers for switched capacitor circuits

Title:
Ring Amplifiers for Switched Capacitor Circuits

Abstract:
In this paper the fundamental concept of ring amplification is introduced and explored. Ring amplifiers enable efficient amplification in scaled environments, and possess the benefits of efficient slew-based charging, rapid stabilization, compression-immunity (inherent rail-to-rail output swing), and performance that scales with process technology. A basic operational theory is established, and the core benefits of this technique are identified. Measured results from two separate ring amplifier based pipelined ADCs are presented. The first prototype IC, a simple 10.5-bit, 61.5 dB SNDR pipelined ADC which uses only ring amplifiers, is used to demonstrate the core benefits. The second fabricated IC presented is a high-resolution pipelined ADC which employs the technique of Split-CLS to perform efficient, accurateamplificationaidedbyringamplifiers.The15-bitADCis implementedina0.18 mCMOStechnologyandachieves76.8dB SNDR and 95.4 dB SFDR at 20 Msps while consuming 5.1 mW, achieving a FoM of 45 fJ/conversion-step .



SAURABH KAURATI

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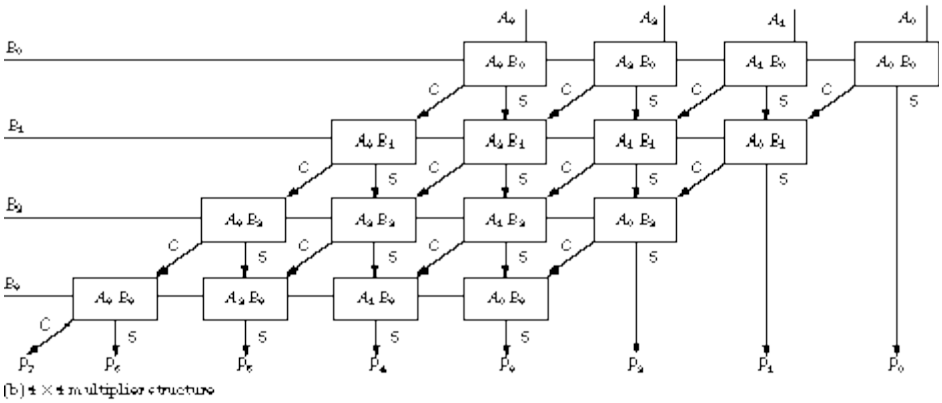
Areas of Interest: Low power digital design

Title: Implementation of 4-bit multiplier using GDI technique

Abstract:
CMOS compatible Gate Diffusion Input (GDI) design technique method enables the implementation of a wide range of complex logic functions using only two transistors. This method is suitable for the design of low-power logic gates, with a much smaller area than Static CMOS and existing PTL techniques. Designed a 4-bit multiplier using GDI technique. Simulations of basic GDI gates under process in 180nm CMOS process are shown and compared to similar CMOS gates. We show that while having the same delay, GDI gates achieve leakage and active power reduction of up to 70% and 50%, respectively.



(b) 4 × 4 multiplier structure

S. R. Kala

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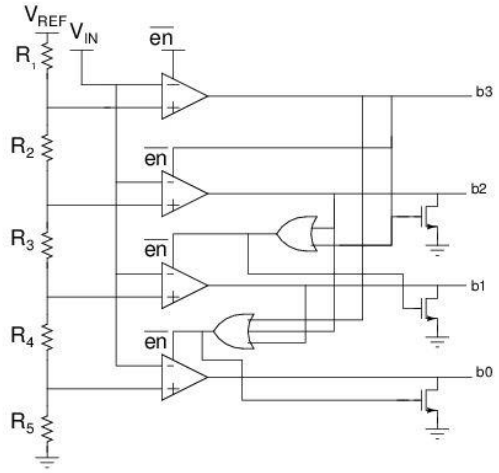
Areas of Interest: Analog to Digital Converters

Title:

Variable Power and Variable Delay ADC for Low-Power Applications

Abstract:

A different type of ADC has been disclosed in this work with variable power and variable delay. The power has been reduced with respect to Flash ADC and maximum delay has been reduced to half as compared to SAR ADC. During the operation of one comparator, other comparators are disconnected from power supply, thereby reducing the power to a great extent. Input voltages near to MSB will have a lesser delay than input voltages near LSB.



Sithara Raveendran

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Areas of Interest: Digital Design, SOC verification, DSP,Analog Design

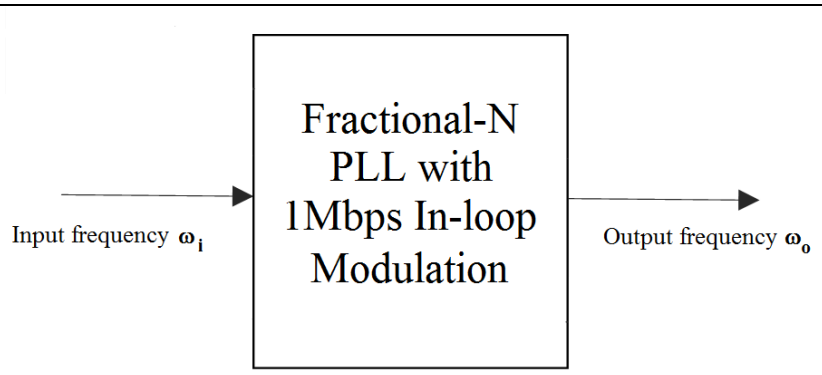
Title:

FPGA Implementation of Wideband 2.4GHz Delta-Sigma Fractional-N PLL with 1Mb/s In-loop Modulation

Abstract:

Implementation of a phase noise cancellation technique that relaxes the fundamental tradeoff between phase noise and bandwidth in conventional delta-sigma fractional –N phase- locked loops (PLLs). It also includes charge pump linearization technique that improves the spurious performance of wideband fractional- PLLs.A delta-sigma modulator is implemented using Verilog and the same is hardware realized on an Xilinx FPGA.

Block Diagram:



SUMESH K.P.

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Areas of Interest: Digital Design, Semiconductor memories and Verilog Coding

Title:

SRAM Based TCAM Architecture Implementation using FPGA

Abstract:

Ternary content addressable memories (TCAMs) perform high-speed lookup operation but when compared with static random access memories (SRAMs), TCAMs have certain limitations such as low storage density, relatively slow access time, low scalability, complex circuitry, and are very expensive. We use the benefits of SRAM by configuring it (with additional logic) to enable it to behave like TCAM This brief proposes a novel memory architecture, named Z-TCAM, which emulates the TCAM functionality with SRAM. Z-TCAM logically partitions the classical TCAM table along columns and rows into hybrid TCAM sub tables, which are then processed to map on their corresponding memory blocks.

Fig 1.Block Diagram of SRAM Based TCAM Architecture