Advt No: NITGOA/DEAN R&C/Project Manpower/2025/001   Date: 30 /06 /2025

Advertisement for the Position of JRF/Project Associate under the R&D Project of C2S scheme, MeiTY, Govt. of India EE-9/2/2021-R&D-E dated 22.05.2023

Applications are invited from interested and highly motivated candidates for the position of Junior Research Fellow (JRF)/Project Associate to work on the R&D project entitled "Design and Development of FPGA Accelerator IP for Deep Neural Network (FAipDNet)" funded under Chips to Startup (C2S) Programme, MeiTY, Govt. of India under the supervision of Dr. Amol D. Rahulkar, Chief Investigator in the Department of Electrical and Electronics Engineering, NIT Goa. The duration of the project is 5 Years. The details of post, essential qualifications and fellowship are as under:

Designation of post	Essential qualifications	Fellowship	Number of post
Junior Research Fellow (JRF)	M.E/M.Tech./M.S or B.E./B.Tech. in relevant specialization of Electrical Engineering/Electronics and CommunicationEngineerng/Instrumentation Engg./ Computer Engineering with minimum of 60% marks (or a minimum of CPGA of 6.5 on a 10-point scale). For SC/ST candidates a minimum 6.0 CGPA on a 10 point scale grading system or 55% marks and A GATE qualification obtained by candidate at some point in time.	Rs. 37,000/- pm + HRA as per norms	01
Project Associate	M.E/M.Tech./M.S OR B.E./B.Tech in relevant specialization of Electrical Engineering/Electronics and CommunicationEngg./Instrumentation Engg./ Computer Engineering with minimum of 60% marks (or a minimum of CPGA of 6.5 on a 10-point scale). For SC/ST candidates a minimum 6.0 CGPA on a 10 point scale grading system or 55% marks	Rs. 25,000/- pm + HRA as per norms	

Job role and skill requirements
- Developing ASIC for Deep Neural Network
- Skilled in Verilog/VHDL, FPGAs, IP integration using Xilinx Vivado, HLS, ASIC design using EDA tools and Python programming
- Good Technical and Communication Skills.

General Terms & Conditions:

1. The duration of post will be initially for one year and which will be extended upto the duration of project based on the satisfactory performance. The fellowship may be terminated if performance of candidate is not satisfactory or as per guidelines received from funding agency.

2. The post created under the C2S Programme, MeitY project is purely on temporary basis and neither MeitY nor the NIT Goa would have liability whatsoever for sustaining temporary staff recruited under the above mentioned project, after its completion/termination.

3. Candidates should apply by filling up the application below. Provide all the details along with self-attested copies of educational certificates, supporting documents and experience should reach to Dr. Amol D. Rahulkar by email at amol.rahulkar@nitgoa.ac.in with cc to tveerakumar@nitgoa.ac.in on or before **22/07/2025** upto **5.00 PM**

4. Subject of the email should be "**Application for JRF/Project Associate under C2S Scheme**", **July 2025.** Only the shortlisted candidates will be informed by e-mail apart from publishing result in the NIT Goa website: www.nitgoa.ac.in along with the date and time of the interview. No other letter will be sent to the correspondence address.

5. Incomplete application forms and forms received after due date will be summarily rejected.

6. The Junior Research Fellow will have option to register for Ph.D. program of institute; the candidate must meet the essential qualifications and qualify written examination & interview of Ph.D. admission of institute.

7. Candidates shall ensure that they are eligible for the position they intend to apply for before appearing for the interview

8. NIT Goa has right to cancel the recruitment for the aforesaid post at any time without providing any clarifications/information.

9. No interim correspondence will be entertained and canvassing in any form will lead to disqualification. No TA/DA will be paid for attending the Interview.

Application for the post of JRF/Project Associate project under C2S Scheme

Title of Project: Design and Development of FPGA Accelerator IP for Deep Neural Network (FAipDNet)

1. Name of the Candidate (BLOCK LETTER):_____

2. Father's Name (BLOCK LETTER): _____

3. Mother's Name (BLOCK LETTER): _____

4. (a) Date of Birth: (DD/MM/YYYY)_____

   (b) Sex (Male/Female/Other):_____

   (c) Marital Status (Married/Single):_____

   (d) Category (SC/ST/OBC/PWD/GEN):_____

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5. (a) Address for Communication: (BLOCKLETTER)

   Contact No. (Mobile):   E-mail ID :

6. Academic Qualification: (Starting from Standard 10 or equivalent Examination)

Name of Exam Passed	Name of the School/College/Institute/ University	Year of Passing	Discipline/ Specialization	Percentage of Marks/ CGPA

7. GATE/NET: Score:_____Rank:_ _____Specialization: _____Year: _____

8. Research Experience details:

Sl. No	Name of position	Organization name and address	Years (From- To)

9. Research Publications (use additional sheet if required)

Total number:

Sl. No	Title of the paper (author/authors)	Journal name (Volume) page no

Note: the first page of the publication should be attached

10. Contact Details of two referees:

	Referee I	Referee II
Name:		
Designation:		
Organization:		
Office Address:		
Office Phone Number:		
Email ID:		

I do hereby declare that the information furnished in this application is true to the best of my knowledge and belief. If selected, I promise to abide by the rules and regulations of the Institute.

Date:

Place: *Signature of the candidate*